

REMARKS

The Official Action mailed May 9, 2005, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on November 14, 2003, and December 17, 2003.

Claims 1-51 are pending in the present application, of which claims 1, 8, 15 and 22-25 of are independent. Dependent claims 19 and 45-51 have been amended to correct informalities and to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

The Official Action rejects claims 1-51 under the doctrine of obviousness-type double patenting over claims 1-44 of U.S. Patent No. 6,242,290 to Nakajima et al. In response to this rejection, a *Terminal Disclaimer* is submitted herewith. Upon filing of this *Terminal Disclaimer*, the claims of the present invention are now believed to be in condition for allowance. Reconsideration and withdrawal of the obviousness-type double patenting rejections are requested.

The Official Action objects to claim 19 for lack of antecedent basis for "said XV group element." In response, claim 19 has been amended to positively recite "an XV group element." Specifically, in claim 19 "wherein one element selected from the group consisting of P, As and Sb is used as said XV group element" has been changed to "wherein said gettering film comprises an XV group element selected from the group consisting of P, As and Sb."

The Official Action objects to claims 45-51 for lack of antecedent basis for "said CMOS circuit" and states that "'a CPU' is not recited in the previous claims, and [does] not further limit the method of fabricating an electronics device in the previous claims" (page 3, Paper No. 20050429). In response, claims 45-51 have been amended to

recite "a CMOS device," which is consistent with the independent claims, and claims 45-51 have been amended to further limit the method of fabricating an electronics device, which is consistent with the form of dependent claims 37-44. Specifically, in claims 45-51, "wherein a CPU comprises said CMOS circuit" has been changed to "wherein said electronics device comprises a CPU comprising said CMOS device."


Reconsideration and withdrawal of the objections are requested.

The Official Action rejects claims 1-7, 22-25 and 31-51 as anticipated by U.S. Patent No. 6,087,245 to Yamazaki et al.

In order to overcome this rejection, a verified English translation of priority application JP 09-205345, filed July 14, 1997, will be filed as soon as it is complete and received from Japan. Since Yamazaki '245 has a filing date of February 11, 1998, which is later than the filing date of JP '345, the Applicants respectfully submit that the rejection under § 102(e) should be overcome. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102(e) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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